Flip-Flops and Related Devices

Multivibrator

Multivibrators, like the familiar sinusoidal oscillators, are circuits with regenerative feedback, with the

difference that they produce pulsed output. There are three basic types of multivibrator, namely the

bistable multivibrator, the monostable multivibrator and the astable multivibrator.

Bistable Multivibrator

A bistable multivibrator circuit is one in which both LOW and HIGH output states are stable.

Irrespective of the logic status of the output, LOW or HIGH, it stays in that state unless a change is

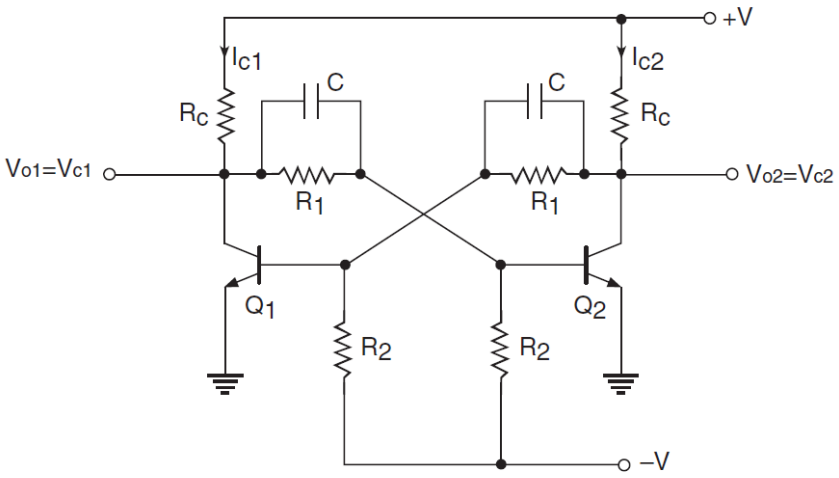


Figure .1 Bistable multivibrator.

Schmitt Trigger

A Schmitt trigger circuit is a slight variation of the bistable multivibrator circuit of Fig. 2. Figure

2 shows the basic Schmitt trigger circuit. If we compare the bistable multivibrator circuit of Fig. 2

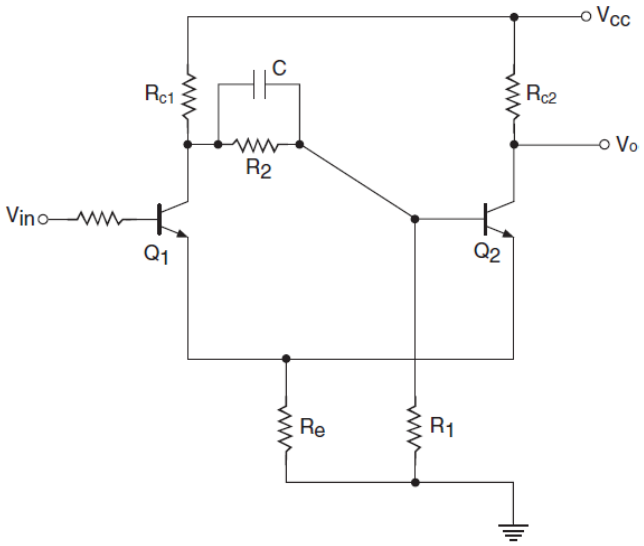


Figure .2 Schmitt trigger circuit.

R-S Flip-Flop

A flip-flop, as stated earlier, is a bistable circuit. Both of its output states are stable. The circuit remains in a particular output state indefinitely until something is done to change that output status. Referring to the bistable multivibrator circuit discussed earlier, these two states were those of the output transistor in saturation (representing a LOW output) and in cut-off (representing a HIGH output). If the LOW and HIGH outputs are respectively regarded as ‘0’ and ‘1’, then the output can either be a ‘0’ or a ‘1’. Since either a ‘0’ or a ‘1’ can be held indefinitely until the circuit is appropriately triggered to go to the other state, the circuit is said to have memory. It is capable of storing one binary digit or one bit of digital information. Also, if we recall the functioning of the bistable multivibrator circuit, we find that, when one of the transistors was in saturation, the other was in cut-off.

This implies that, if we had taken outputs from the collectors of both transistors, then the two outputs would be complementary.

In the flip-flops of various types that are available in IC form, we will see that all these devices offer complementary outputs usually designated as Q and Q'

The R-S flip-flop is the most basic of all flip-flops. The letters 'R' and 'S' here stand for RESET and SET. When the flip-flop is SET, its Q output goes to a '1' state, and when it is RESET it goes to a '0' state. The Q' output is the complement of the Q output at all times.

R-S *Flip-Flop with Active LOW Inputs*

Thus, R and S are active when LOW. The term CLEAR input is also used sometimes in place of RESET. The operation of the R-S flip-flop of Fig. 10.17(a) can be summarized as follows:

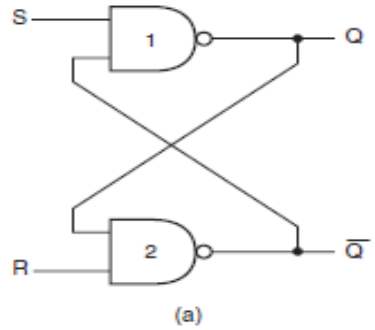
1. SET=RESET= 1 is the normal resting condition of the flip-flop. It has no effect on the output state of the flip-flop. Both Q and Q outputs remain in the logic state they were in prior to this input condition.

2. SET = 0 and RESET = 1 sets the flip-flop. Q and Q respectively go to the '1' and '0' state.

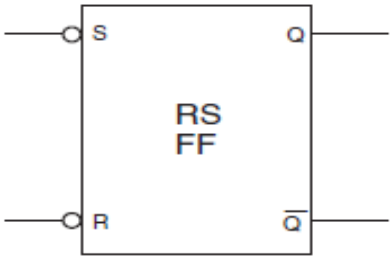
3. SET =1 and RESET =0 resets or clears the flip-flop. Q and Q respectively go to the '0' and '1' state.

4. SET = RESET = 0 is forbidden as such a condition tries to set (that is, Q = 1) and reset (that is, Q = 1) the flip-flop at the same time. To be more precise, SET and RESET inputs in the R-S flip-flop cannot be active at the same time.

The R-S flip-flop of Fig. 10.17(a) is also referred to as an R-S latch. This is because any combination at the inputs immediately manifests itself at the output as per the truth table.



(a)

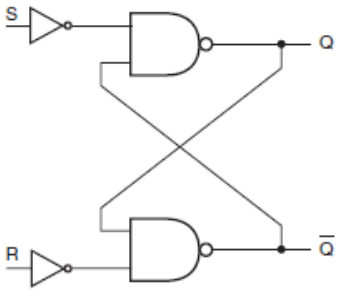


(b)

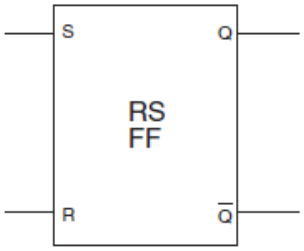
Operation Mode	S	R	Q_{n+1}
No change	1	1	Qn
SET	0	1	1
RESET	1	0	0
Forbidden	0	0	—

(c)

Figure 3 R-S flip-flop with active LOW inputs.



(a)



(b)

Operation Mode	S	R	Q_{n+1}
No change	0	0	Q_n
SET	1	0	1
RESET	0	1	0
Forbidden	1	1	—

(c)

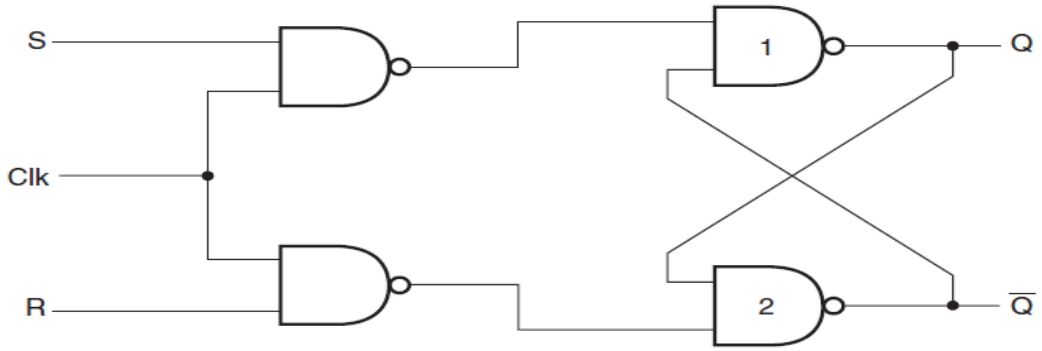
Figure 4 R-S flip-flop with active HIGH inputs.

Clocked R-S *Flip-Flop*

In the case of a clocked R-S flip-flop, or for that matter any clocked flip-flop, the outputs change states as per the inputs only on the occurrence of a clock pulse. The clocked flip-flop could be a level-triggered one or an edge-triggered one. The two types are discussed in the next section. For the time being, let us first see how the flip-flop of the previous section can be transformed into a clocked

flip-flop. Figure 4 shows the logic implementation of a clocked flip-flop that has active HIGH inputs. The function table for the same is shown in Fig. 4 and is self-explanatory.

The basic flip-flop is the same as that shown in Fig. 4. The two NAND gates at the input have been used to couple the R and S inputs to the flip-flop inputs under the control of the clock signal. When the clock signal is HIGH, the two NAND gates are enabled and the S and R inputs are passed on to flip-flop inputs with their status complemented. The outputs can now change states as per the status of R and S at the flip-flop inputs. For instance, when S = 1 and R = 0 it will be passed on as 0 and 1 respectively when the clock is HIGH. When the clock is LOW, the two NAND gates produce a '1' at their outputs, irrespective of the S and R status. This produces a logic '1' at both inputs of the flip-flop, with the result that there is no effect on the output states.



(a)

S	R	Clk	Q_{n+1}
0	0	0	Q_n
0	0	1	Q_n
0	1	0	Q_n
0	1	1	0
1	0	0	Q_n
1	0	1	1
1	1	0	Q_n
1	1	1	Invalid

(b)

Figure 5 Clocked R-S flip-flop with active HIGH inputs.